

EXPRESSMAIL NO. EL755725122US
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Rakesh Malik and Puneet Goel
International
Application No. : PCT/SG98/00082
U.S. Application No.: 09/807,500
International Filing
Date : October 13, 1998
Priority Date Claimed: October 13, 1998
For : AREA EFFICIENT REALIZATION OF COEFFICIENT
ARCHITECTURE FOR BIT-SERIAL FIR, IRR FILTERS AND
COMBINATIONAL/SEQUENTIAL LOGIC STRUCTURE
WITH ZERO LATENCY CLOCK OUTPUT
Docket No. : 851663.422USPC
Date : September 17, 2001

Box PCT
Commissioner for Patents
Washington, DC 20231

RESPONSE TO NOTIFICATION MISSING REQUIREMENTS UNDER 35 U.S.C. 371 IN
THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

Commissioner for Patents:

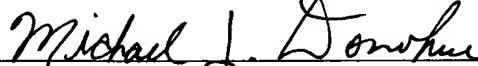
In response to the Notification of Missing Requirements please note that the Response was filed on June 11, 2001. For your reference, copies of the following documents are attached:

<u>X</u>	Copy of Notification of Missing Requirements
<u>X</u>	Copy of Transmittal Letter
<u>X</u>	Copy of Declaration and Power of Attorney
<u>X</u>	Copy of Recordation Form Cover Sheet
<u>X</u>	Copy of Assignment
<u>X</u>	Copy of Express Mail Receipt
<u>X</u>	Copy of Postcard Stamped by PCT/PTO

Respectfully submitted,

Rakesh Malik and Puneet Goel

Seed Intellectual Property Law Group PLLC


Michael J. Donohue
Registration No. 95,859

Enclosure:

Postcard
851663.422USPC/215848_1.DOC